ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 8, August 2015

Design and Implementation of a Digital Accumulator for the Phase Coherent Radio Pulse Signal using FPGA

Dr.Kamal Aboutabikh[1], Dr.Mansour Babiker Idris[2], Dr.Ibrahim Haidar[3]

Faculty of Engineering, Kassala university, Kassala, Sudan[1,2]

Faculty of Engineering , Cordoba Private University, Kamashli, Syria[3]

Abstract: In this paper, we introduce a practical mechanism of forming and accumulating phase coherent radio pulses signal in presence of additive white Gaussian noise (AWGN) by a digital pulses accumulator using FPGA to improve the signal-to-noise ratio (SNR) through designing a direct digital frequency synthesizer (DDFS) to synthesize the phase coherent radio pulses signal in presence of AWGN by digital pseudo noise generator (DPNG) at different SNR_{inp} and design a digital accumulator for 20 phase coherent radio pulses, and this maximizes SNR_{out} by 13 dB using Quartus II 9.1 design environment.

Keywords: AWGN ,Radio Pulse, DDFS, DPNG, Digital Accumulator ,FPGA.

I. INTRODUCTION

To maximize the signal to noise ratio(SNR) on the output of the radio receiver, the different various digital filtering algorithms are used, such that:

- Algorithms of binary phase code modulation (BPCM) [1] for Direct spread spectrum systems (DSSS) signals and algorithms of linear frequency modulation (LFM) signal [2] .
- Algorithms of digital matched filter (DMF) [3] for all kinds of receivers.
- Algorithm of digital accumulating for phase coherent radio signal [4].

The accumulating principle depends on using digital delay lines consist of sets of parallel-parallel shift registers, the number of registers depends on the ratio of pulses period to samples period (T/T_{sam}) and serial connected with each other to perform one repetition period delay, then these sets are serial connected with each other according to the number of accumulating times (N) and the signal samples are added from output every set to get signal to noise ratio ($N^{0.5}$) by voltage and (N) by power.

The needed number of parallel-parallel shift registers to achieve the accumulating number N is [5]:

$$M = N.\left(\frac{T}{Tsam}\right) \qquad (1)$$

Then, we get an increasing in SNR_{out} by power with amount:

$$G = 10\log(N) \qquad (2)$$

So the accumulating time equals to:

$$Taccum = N.T \qquad (3)$$

- For samples period $T_{sam} = 0.1\mu s$, the pulses repetition period $50\mu s$, and N=10000, we need a total number of shift registers equals to :

$$M = N.\left(\frac{T}{Tsam}\right) = 10000 * \left(\frac{50}{0.1}\right) = 5000000\ SR$$

Then, we get an increasing in SNR_{out} by power with amount:

$$G = 10\log(N) = 10\log(10000) = 40\ dB$$

So the accumulating time equals to:

$$Taccum = N.T = 10000 * 50 = 500000\mu s = 0.5\ s$$

- Today, this process is possible because of FPGA chips available with high integrated degree and work within the real time of processing.
- The results of accumulator work are studied by using a digital work bench and digital oscilloscope for input and output signals due to several values of SNR_{inp}.
- In this research, we discuss the mechanism of phase coherent radio pulses accumulating using a digital accumulator designed on a digital programmable device (Cyclone II EP2C70F896C6 FPGA from ALTERA) placed on education and development board DE2-70 [6].
- The values of SNR, T_{accum}, the number of parallel shift registers and ($N^{0.5}$) are shown in table (1), we note that SNR can be increased to a value 50 dB if the FPGA has high hardware capabilities.

Table (1) SNR values for $F_{sam} = 10\ MHz$, $T = 50\ \mu s$

N	$N^{0.5}$	Nom SR	T_{accum}(ms)	SNR_{out}(dB)
20	4.5	10000	1	13
100	10	50000	5	20
1000	31.6	500000	50	30
10000	100	500000	500	40
100000	316	5000000	5000	50

II. RESEARCH MATERIALS AND ITS WAYS

The diagram of research and study for the digital accumulator is shown on the Fig.1 for accumulating 20 pulses and it consists of direct digital frequency synthesizer (DDFS) with digital pulse modulator to synthesis the phase coherent radio pulse and digital pseudo noise generator (DPNG) to synthesis additive white Gaussian noise (AWGN), adder to add the radio pulses

DOI 10.17148/IJARCCE.2015.48107

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 8, August 2015

with AWGN and digital accumulator to accumulate 20 phase coherent pulses on the IF frequency, two DAC of 8 bits to transform the signals from digital form to analog form before and after accumulating, PC computer to link DE2-70 board via USB and inject the design in the Cyclone II EP2C70F896C6 FPGA chip, and digital oscilloscope GDS-1052U connected to PC via USB to show the input and output signals of the accumulator in time domain due to various SNR_{inp} cases. Fig.2 shows the block diagram of the search and study system with Quartus II 9.1 design environment.

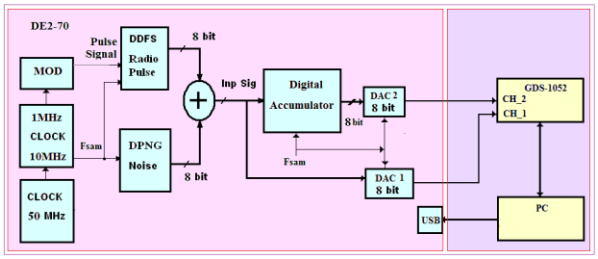

Fig.1: The search and study diagram of the digital accumulator

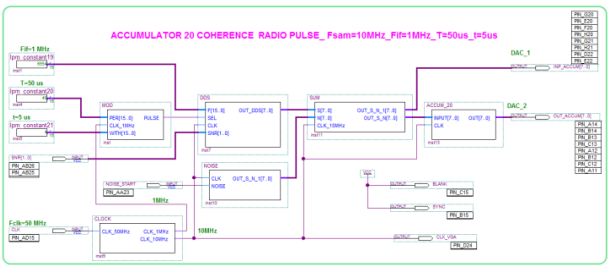

Fig.2: The block diagram of the search and study system with Quartus II 9.1 design environment

III. THE RADIO PULSES SIGNAL SPECIFICATIONS

- Signal type: phase coherent radio pulses with AWGN.
- Synthesizing technique: DPNG, DDFS.
- Carrier frequency IF: $F_{IF} = 1MHz$.
- Samples frequency: $F_{sam} = 10MHz, T_{sam} = 100ns$.
- Pulse width: $\tau = 5\mu s$.
- Pulses period: $T_0 = 50\mu s$.
- The number of radio signal periods during the pulse width [7]:

$$N_{PER} = \tau_s / T_{IF} = \tau_s . F_{IF} \qquad (4)$$

$$N_{PER} = \tau_s / T_{IF} = 5 * 1 = 5$$

Where: ($T_{IF} = 1/F_{IF}$) the high frequency signal period for radio pulse modulation.

- Algorithm for generation for the phase coherent radio pulse signal shown in Fig .3 where using DDFS with code frequency (L_{IF}) for (F_{IF}) given by the following relation[8]:

$$L_{IF} = \frac{2^n . F_{IF}}{F_{sam}} \qquad (5)$$

Where :n is the length of the phase accumulator DDFS ,in bits.

For $F_{IF} = 1MHz$, $F_{sam} = 10MHz$ and n=32bits ,code frequency:

$$L_{IF} = \frac{2^n . F_{IF}}{F_{sam}} = \frac{2^{32} * 1}{10} = 429496730$$

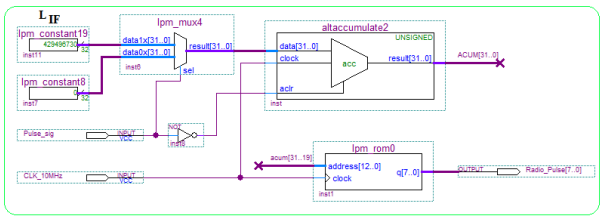

Fig.3 Algorithm generation for the phase coherent radio pulse signal using DDFS

IV. THE DIGITAL ACCUMULATOR SPECIFICATIONS

- Signal input: radio pulses of pulse modulation on AWGN background.
- The ratio $SNR_{inp} = 1/1, 1/2, 1/3, 1/4$.
- The length of processing word for the input signal is signed 8-bits.
- The number of delay stages is 20.
- The single delay step: $\delta\tau = Z = T_{sam} = 100ns$.
- The number of accumulating pulses is $N = 20$.
- The number of delay stages for one period [5]:

$$D_D = \frac{T_0}{T_{sam}} \qquad (6)$$

$$D_D = \frac{T_0}{T_{sam}} = \frac{50000}{100} = 500$$

Every delay stage of one period D_D consists of 500 parallel shift registers (lpmshiftreg 0…..lpmshiftreg 499) of 8bits, all delay stages for the one period are serial connected according the Fig 4.

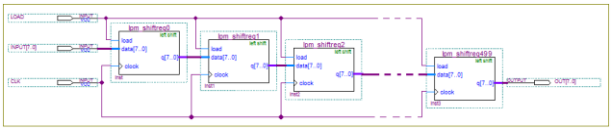

Fig.4: The number of shifting stages D_D for on period delay T

-For 20 periods, the number of delay stages:

$$D_{D(N)} = N . D_D \qquad (7)$$

$$D_{D(N)} = N . D_D = 20 * 500 = 10000$$

- The parallel shift registers number of 8-bits is 10000SR.
- Adder has 20 inputs of 8-bits, and one output of 13bits.
- Different logic and mathematic operations (AND, NOT, XOR, etc).
- The capacity of used memory is 3x7bit.

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 8, August 2015

- Filtering degree is M=20.
- Filter coefficients:

$$a_0 = 1, a_1 = 1, a_2 = 1, a_3 = 1, \ldots\ldots a_{20} = 1.$$

- Processing algorithm: digital convolution algorithm in time domain on-line.
- Processing velocity is 20 adding, shifting and conversion operations through 50 ns which equal 1000 million operations per second, this equivalent to 1 GHz processor clock frequency, so the processing is done simultaneously on-line.
- Matched processing gain factor is:

$$K_{MF} = SNR_{out} / SNR_{inp} \Rightarrow K_{MF}(dB) = 10 \log N = 10 \log 20 = 13dB$$

- Fig.5 shows a digital accumulating algorithm of samples number (length) for the reference signal is M=20.

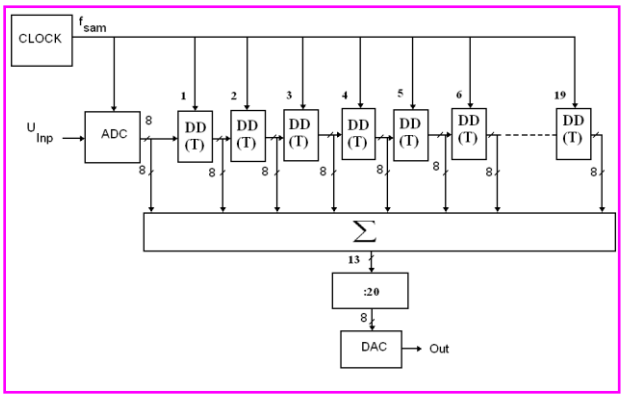

Fig.5: The digital accumulating algorithm of length M=20

V. PRACTICAL DESIGN RESULTS FOR THE DIGITAL ACCUMULATOR

The practical design results of the accumulator in time domain for input and output signals were taken by digital oscilloscope of type GDS-1052U .

Fig.6 shows the input and output signals of the accumulator without the noise effect.

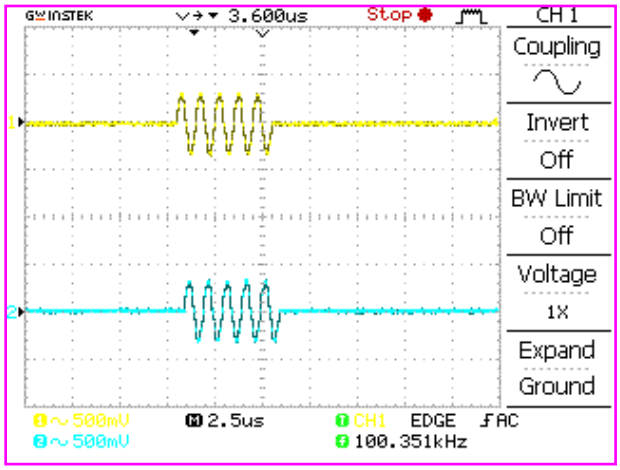

Fig.6: The input and output signals of the accumulator without the noise effect

Fig.7 shows the input and output signals under noise effect and $SNR_{inp} = 1/1$.

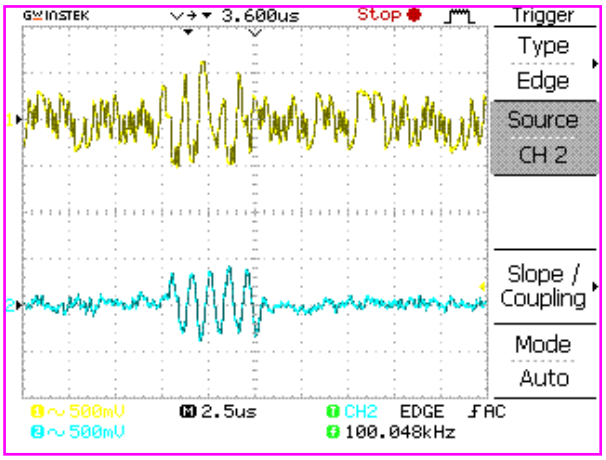

Fig.7: The input and output signals under noise effect and $SNR_{inp} = 1/1$

Fig.8 shows the input and output signals under noise effect and $SNR_{inp} = 1/2$.

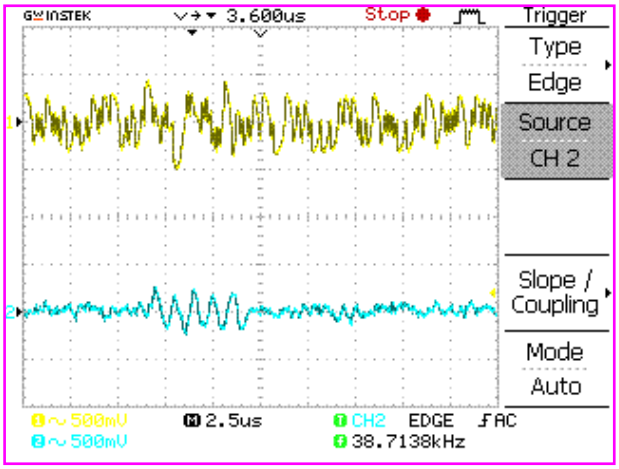

Fig.8: The input and output signals under noise effect and $SNR_{inp} = 1/2$

Fig.9 shows the input and output signals under noise effect and $SNR_{inp} = 1/3$.

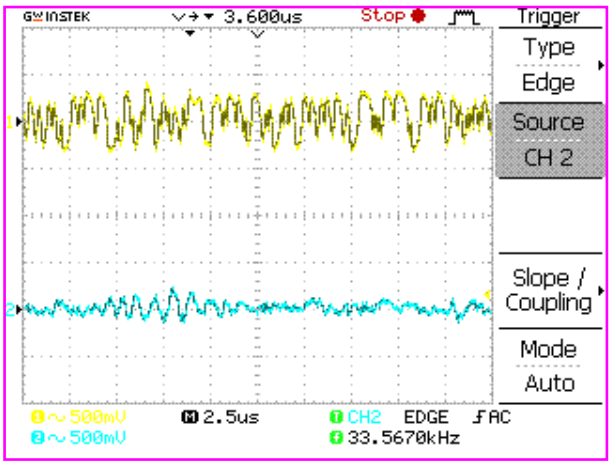

Fig.9: The input and output signals under noise effect and $SNR_{inp} = 1/3$

DOI 10.17148/IJARCCE.2015.48107

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
Vol. 4, Issue 8, August 2015

Fig.10 shows the input and output signals under noise effect and $SNR_{inp} = 1/4$.

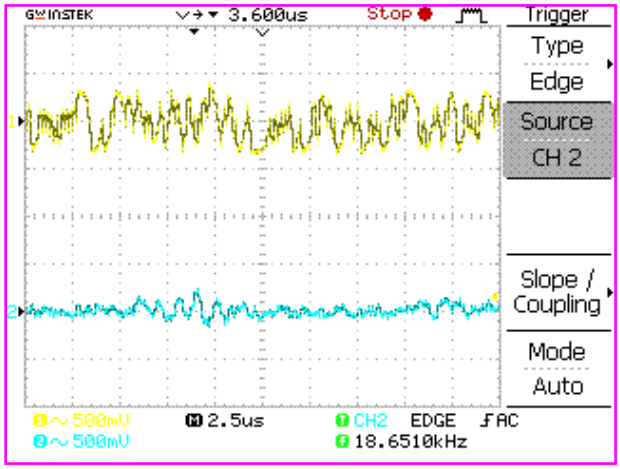

Fig.10: The input and output signals under noise effect and $SNR_{inp} = 1/4$

VI. CONCLUSION

Depending on the previous results, the digital accumulator successfully maximizes the ratio SNR, also it may be improve this ratio through increasing the number of accumulator stages by using the modern digital FPGA chips.

In this research, the simulator of the correlated phase radio pulses signal using DDFS and the noise interference signals using DPNG are successfully designed . From the execution practical experiments, this kind of accumulators can be used in modern digital processing devices with other kinds of SNR maximizing algorithms.

To develop the search in future, the education and development boards can be used with digital chips which have a big number of digital functions to achieve better SNR of 50 dB.

REFERENCES

[1] C. S.Rawat, Deepak Balwani , DiptiBedarkar , JeetanLotwani, HarpreetKaurSaini , Implementation of Barker Code and Linear Frequency Modulation Pulse Compression Techniques in MatlabInternational Journal of Emerging Technology and Advanced Engineering, Volume 4, Issue 4, April 2014(105-111).

[2] ZoranGolubicic, Slobodan Simic c , Aleksa J. Zejak, Design and FPGA implementation of digital pulse compression for band-pass Radar signals, Journal of Electrical Engineering, VOL. 64, NO. 3, 2013, 191–195.

[3] Introduction to matched filters John C. Bancroft CREWES Research Report . Volume 14 (2002).

[4] H. A. Said**,** A. A. El-Kouny, A. E. El-Henawey, Design and Realization of Digital Pulse Compression in Pulsed Radars Based on Linear Frequency Modulation (LFM) Waveforms Using FPGA ,International Conference on Advanced Information and Communication Technology for Education (ICAICTE 2013).

[5] Dr. Kamal Aboutabikh, Dr. Ibrahim Haidar , DIGITAL COMPRESSING OF A BPCM SIGNAL ACCORDING TO BARKER CODE USING FPGA, International Journal of Technical Research and Applications e-ISSN: 2320-8163, www.ijtra.com Volume 3, Issue 4 (July-August 2015), PP. 73-79

[6] www.altera.com.

[7] C. D. Rawat and Anuja D. Sarate ,modern signal processing in Radar ,International ,International Journal of Application or Innovation in Engineering & Management (IJAIEM) Web Site: www.ijaiem.org Email: editor@ijaiem.org ,ISSN 2319 – 4847 Special Issue for International Technological Conference-2014.

[8] GOLDBERG B. 1999- Digital Frequency Synthesis Demystified, LLH Technology Publishing, united states, 334.

BIOGRAPHIES

Dr Kamal Aboutabikh holds a PhD in communication engineering in 1988 from the USSR , university of communication in Leningrad , holds a degree assistant professor in 2009 from Aleppo university. Lecturer at Department of Biomedical Engineering, Al Andalus University For Medical Sciences-Syria,Tishreen University-Syria ,Corduba Private University- Syria and Kassal University-Sudan. Publish a lot of research in the field of digital communication and digital signal processing in the universities of Syria and in the European and Indian journals. Working in the field of programming FPGA by using VHDL and design of Digital Filters.

Dr Mansour Babiker Idris holds a PhD in power system engineering in 2011 from the Karary University-Sudan. Assistant professor since 2011 from Red Sea University. Lecturer at Read Sea University (2006-2011), Lecturer at Misurata University-Lybia (2012-2013), Assistant professor at Kassala University (2013-now). Dean Faculty of Engineering (2013-now). Publish a lot of research in the field power systems and stability. Working in the field of programming FPGA by using VHDL and design of Digital Filters.